**Several Problems and solutions**

**Question1 :**

**Function 1 design Verilog code:**

***fun\_1. v:*** 𝒇𝟏 = (𝒙𝟏 + 𝒙𝟐’) + 𝒙𝟐. 𝒙𝟑’ + 𝒙𝟑’.𝒙𝟒’+ (𝒙𝟏 + 𝒙𝟒’)

………………………………………………………………….

`timescale 1ns / 1ps

module fun\_1(

input x1,

input x2,

input x3,

input x4,

output f1

);

assign f1=(x1|(~x2)) | (x2&(~x3)) | ((~x3)&(~x4)) | (x1|(~x4));

endmodule

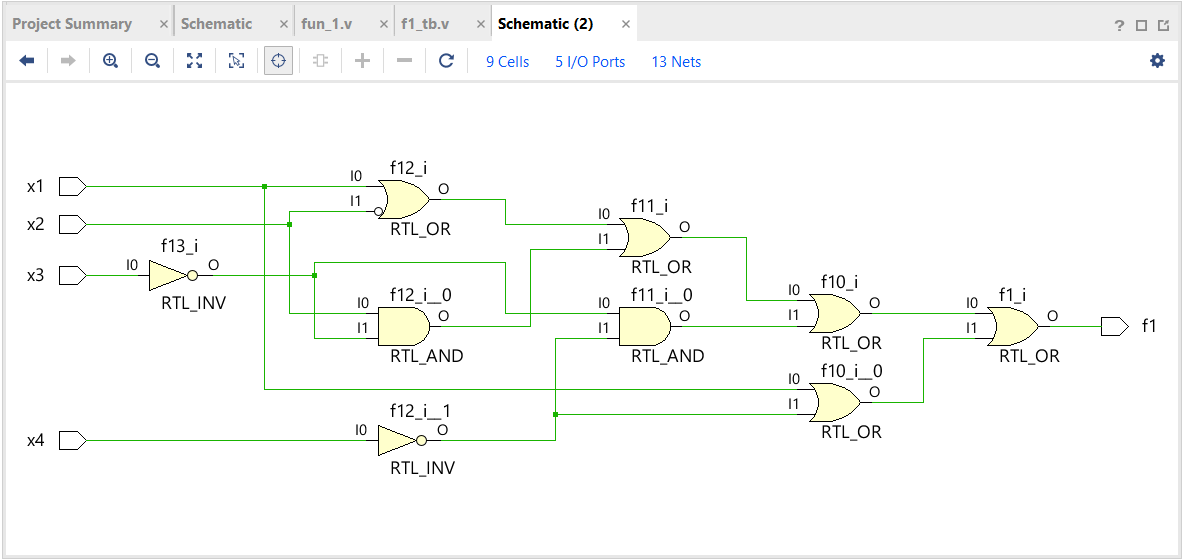
***Schematic Diagram:***

Figure 1: Schematic diagram for Function 1

**Testbench for fun\_1.v:**

***f1\_tb. v:***

………………………………………………………………..

`timescale 1ns / 1ps

module f1\_tb;

reg x1;

reg x2;

reg x3;

reg x4;

wire f1;

fun\_1 uut(

.x1(x1),

.x2(x2),

.x3(x3),

.x4(x4),

.f1(f1)

);

initial begin

x1=0; x2=0; x3=0; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=0; x2=0; x3=0; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=0; x2=0; x3=1; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=0; x2=0; x3=1; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=0; x2=1; x3=0; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=0; x2=1; x3=0; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=0; x2=1; x3=1; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=0; x2=1; x3=1; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=1; x2=0; x3=0; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=1; x2=0; x3=0; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=1; x2=0; x3=1; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=1; x2=0; x3=1; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=1; x2=1; x3=0; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=1; x2=1; x3=0; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=1; x2=1; x3=1; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=1; x2=1; x3=1; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

$finish;

end

endmodule

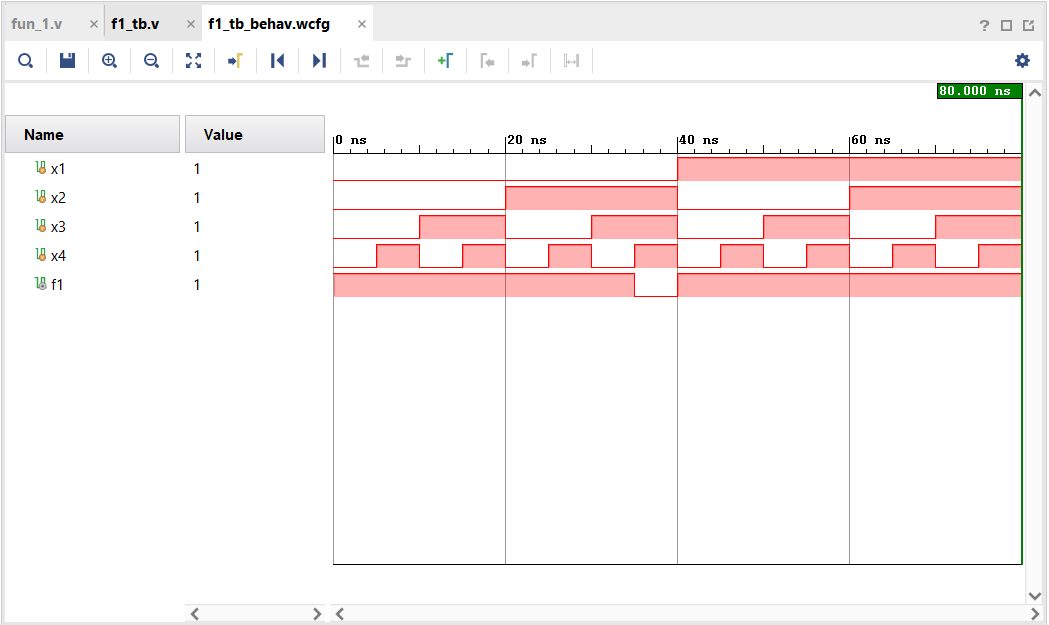
**OUTPUT:**

Figure 2: Output waveform for function 1

**Function 2 design Verilog code:**

***fun\_2. v:***

………………………………………………………………….

`timescale 1ns / 1ps

module fun\_2(

input x1,

input x2,

input x3,

input x4,

output f2

);

assign f2 = (x1 & ~x2)&(x2 | ~x3)&(~x3 | ~x4)&(x1 & ~x4);

endmodule

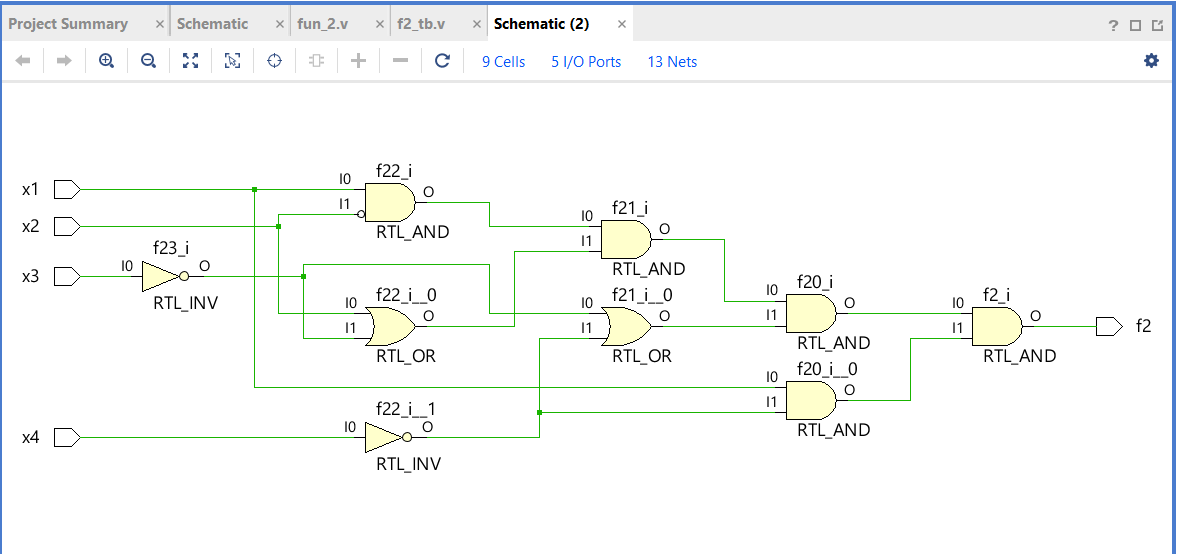
***Schematic Diagram:***

Figure 3: Schematic diagram for Function 2

**Testbench for fun\_2.v:**

***F2\_tb. v:***

………………………………………………………………..

`timescale 1ns / 1ps

module f2\_tb;

reg x1;

reg x2;

reg x3;

reg x4;

wire f2;

fun\_2 uut(

.x1(x1),

.x2(x2),

.x3(x3),

.x4(x4),

.f2(f2)

);

initial begin

x1=0; x2=0; x3=0; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=0; x2=0; x3=0; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=0; x2=0; x3=1; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=0; x2=0; x3=1; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=0; x2=1; x3=0; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=0; x2=1; x3=0; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=0; x2=1; x3=1; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=0; x2=1; x3=1; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=1; x2=0; x3=0; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=1; x2=0; x3=0; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=1; x2=0; x3=1; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=1; x2=0; x3=1; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=1; x2=1; x3=0; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=1; x2=1; x3=0; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=1; x2=1; x3=1; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=1; x2=1; x3=1; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

$finish;

end

endmodule

**OUTPUT:**

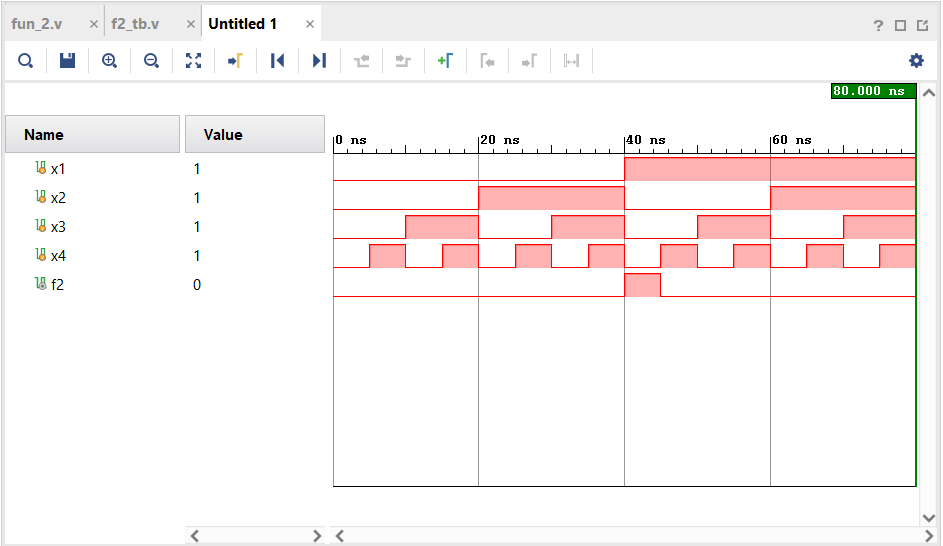


Figure 4: Output waveform for function 2

**Question 2 design Verilog code:**

F(x1,x2,x3,x4)= =x2x4+x1’x3x4+x1’x2’x3’x4’

***min\_f. v:***

………………………………………………………………..

`timescale 1ns / 1ps

module min\_f(

input x1,

input x2,

input x3,

input x4,

output f1

);

assign f1 = (x2&x4) | (~x1&x3&x4) | (~x1& ~x2 & ~x3 & ~x4);

endmodule

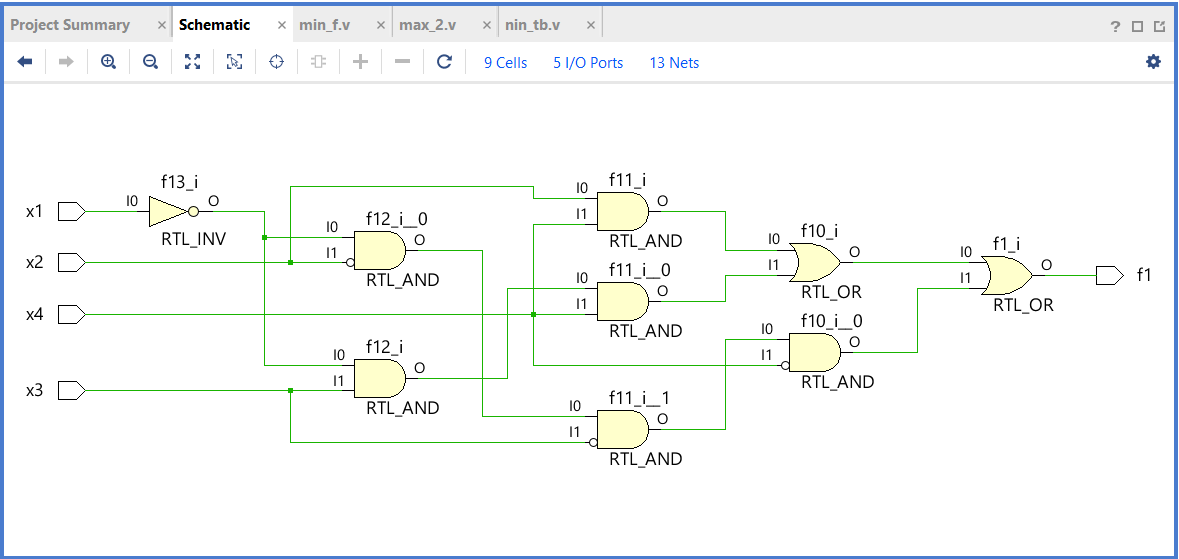
***Schematic Diagram:***

Figure 5: schematic diagram for question 2

**Testbench for min\_f.v:**

***min\_tb. v:***

………………………………………………………………..

`timescale 1ns / 1ps

module min\_tb;

reg x1;

reg x2;

reg x3;

reg x4;

wire f1;

min\_f uut(

.x1(x1),

.x2(x2),

.x3(x3),

.x4(x4),

.f1(f1)

);

initial begin

x1=0; x2=0; x3=0; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=0; x2=0; x3=0; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=0; x2=0; x3=1; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=0; x2=0; x3=1; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=0; x2=1; x3=0; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=0; x2=1; x3=0; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=0; x2=1; x3=1; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=0; x2=1; x3=1; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=1; x2=0; x3=0; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=1; x2=0; x3=0; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=1; x2=0; x3=1; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=1; x2=0; x3=1; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=1; x2=1; x3=0; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=1; x2=1; x3=0; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=1; x2=1; x3=1; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

x1=1; x2=1; x3=1; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f1 = %b", x1, x2, x3, x4, f1);

$finish;

end

endmodule

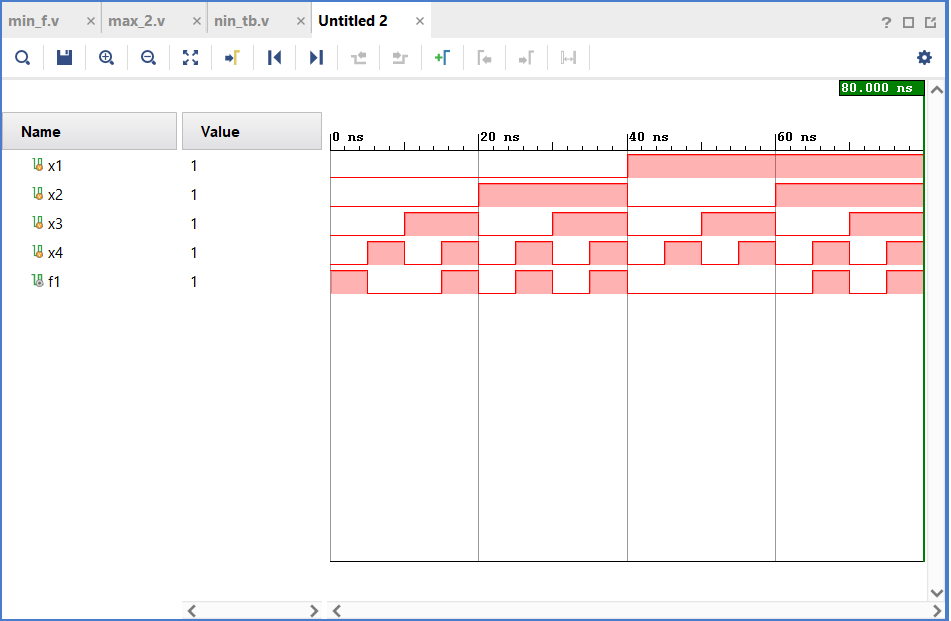
**OUTPUT:**

Figure 6: timing diagram of question 2

**Question 3 design Verilog code:**

F(x1,x2,x3,x4)= =(x1+x4’)(x2’+x4’)

***max\_2. v:***

………………………………………………………………..

`timescale 1ns / 1ps

module max\_2(

input x1,

input x2,

input x3,

input x4,

output f2

);

assign f2= (x1| ~x4) & (~x2 | ~x4);

endmodule

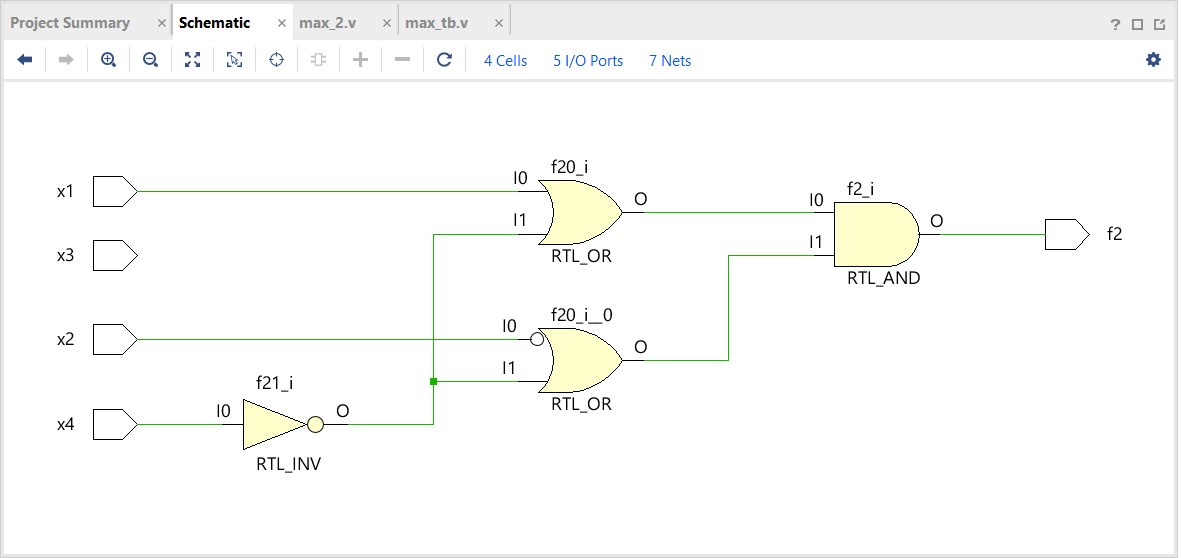


Figure 7: schematic diagram for question 3

**Testbench for max\_2.v:**

***max\_tb. v:***

………………………………………………………………..

`timescale 1ns / 1ps

module max\_tb;

reg x1;

reg x2;

reg x3;

reg x4;

wire f2;

max\_2 uut(

.x1(x1),

.x2(x2),

.x3(x3),

.x4(x4),

.f2(f2)

);

initial begin

x1=0; x2=0; x3=0; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=0; x2=0; x3=0; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=0; x2=0; x3=1; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=0; x2=0; x3=1; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=0; x2=1; x3=0; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=0; x2=1; x3=0; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=0; x2=1; x3=1; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=0; x2=1; x3=1; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=1; x2=0; x3=0; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=1; x2=0; x3=0; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=1; x2=0; x3=1; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=1; x2=0; x3=1; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=1; x2=1; x3=0; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=1; x2=1; x3=0; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=1; x2=1; x3=1; x4=0;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

x1=1; x2=1; x3=1; x4=1;

#5 $display("x1 = %b, x2 = %b, x3 = %b, x4 = %b, f2 = %b", x1, x2, x3, x4, f2);

$finish;

end

endmodule

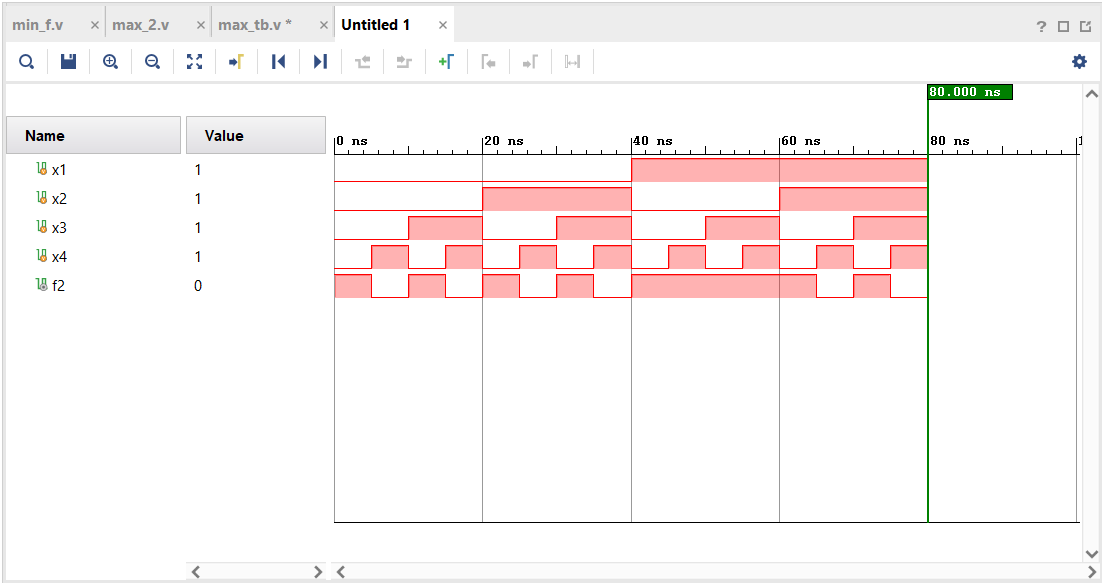
**OUTPUT:**

Figure 8: timing diagram of question 3